SPECIFICATION

At page 3, line 32, through page 4, line 16, please amend the text as follows:

In accordance with another embodiment of the presently claimed invention, a decision feedback equalizer with dynamic feedback control for adaptively controlling a pre-slicer data signal that is sliced to provide a post-slicer data signal includes signal combiner means, signal slicer means, decision feedback means and signal differentiator means. ~~First~~ A first signal combiner means is for combining a feedback signal and an input signal representing a plurality of data and generating a pre-slicer signal. The signal slicer means is for slicing the pre-slicer signal and generating a post-slicer signal indicative of the plurality of data. The decision feedback means is for controlling signal timing by feeding back the post-slicer signal in response to a control signal and generating the feedback signal. ~~Second~~ A second signal combiner means is for combining the pre-slicer and post-slicer signals and generating a difference signal indicative of a difference between the pre-slicer and post-slicer signals. The signal differentiator means includes a selected signal delay and is for differentiating and delaying the input signal and generating a resultant signal, wherein respective portions of the resultant signal are delayed relative to corresponding portions of the input signal by the selected signal delay. ~~Third~~ A third signal combiner means is for combining the difference signal and the resultant signal and generating the control signal, wherein the selected signal delay is selected such that the control signal has a substantially zero AC signal component.

At page 7, lines 3-24, please amend the text as follows:

The subject matter discussed herein, including the presently claimed invention, is compatible and suitable for use with the subject matter disclosed in the following copending, commonly assigned patent applications (the disclosures of which are incorporated herein by reference): U.S. patent application 10/117,293, filed April 5, 2002, and entitled "Compensation Circuit For Reducing Intersymbol Interference Products Caused By Signal Transmission Via Dispersive Media"; U.S. patent application 10/179,689, filed June 24, 2002, and entitled "Crosstalk Compensation Engine For Reducing Signal Crosstalk Effects Within A Data Signal"; U.S. patent application 10/244,500, filed September 16, 2002, and entitled "Compensation Method For Reducing Intersymbol Interference Products Caused By Signal Transmission Via Dispersive Media"; U.S. patent application 10/290,674, filed November 8, 2002, and entitled "Compensation Circuit And Method For Reducing Intersymbol Interference Products Caused By Signal Transmission Via Dispersive Media"; U.S. patent application 10/290,993, filed November 8, 2002, and entitled "Adaptive Signal Equalizer With Adaptive Error Timing And Precursor/Postcursor Configuration Control"; ~~U.S. patent application 10/___,___, filed _____, ____, 2002 [atty. docket S1471.00009],~~ U.S. patent application 10/321,893, filed December 17, 2002, and entitled "Adaptive Signal Latency Control For Communications Systems Signals"; ~~U.S. patent application 10/___,___, filed _____, ____, 2002 [atty. docket S1471.00011],~~ U.S. patent application 10/321,876, filed December 17, 2002, and entitled "Adaptive Signal Equalizer With Adaptive Error Timing And Precursor/Postcursor Configuration Control"; and U.S. patent application 10/179,996, filed June, 24, 2002, and entitled "Programmable Decoding of Codes of Varying Error-Correction Capability".